PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Eric B. KUSHNICK | Art Unit: 2116

Application No: 09/824,898 | Examiner: Tse W. Chen

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For: HIGH RESOLUTION CLOCK SIGNAL GENERATOR

BRIEF ON BEHALF OF APPELLANT

COMMISSIONER FOR PATENTS
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Sir:

Real Party In Interest

Credence Systems Corporation

Related Appeals and Interferences

None

Status of Claims

Claims 1-14 and 17-38 are pending.

Claims 17-19 are allowed.

Claims 1-8, 11, 20-27, 30, 34, 35 are rejected

Claims 9, 10, 12-14, 28, 29, 31-33 and 36-38 are objected to as relying on rejected base claims.

Claims 15 and 16 have been withdrawn.

Claims 1-8, 11, 20-27, 30, 34 and 35 are appealed.

Status of Amendments

No amendments are pending.

Summary of Claimed Subject Matter

Claim 1

Independent claim 1 is best understood with reference to the applicant's FIG. 5. The invention as recited in claim 1 is an apparatus for generating pulses of a third pulse sequence (CLOCK') in response to pulses of a periodic first pulse sequence (ROSC) having a period T_P. Claim 1 recites that the apparatus comprises

first means **(item 54, specification paragraph 44 and FIG. 8)** for generating each pulse of a second pulse sequence (CLOCK) in response to a separate pulse of the first pulse sequence (ROSC) with a first delay adjustable by first control data (SW(A)) with a resolution of T_P/N over a first range substantially wider than T_P/M, wherein M and N are differing integers greater than one;

second means **(item 56, specification paragraphs 42 and 43 and FIG. 7)** for generating each pulse of the third pulse sequence (CLOCK') in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data (SW(B)) with a resolution of T_P/M over a second range substantially wider than T_P/N; and

a programmable sequencer **(item 58, specification paragraphs 42 and 44 and FIG. 5)** for changing a magnitude of the first control data (SW(A)) and the second control data (SW(B)) in response to each pulse of the first pulse sequence (ROSC) such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner.

The invention recited in claim 1 can, for example, produce a periodic output signal (CLOCK') having a period that differs from that of a periodic input signal (ROSC) that it uses as a timing reference. The period of the CLOCK' signal can be adjusted by adjusting the repetitive first and second control data patterns produced by programmable sequencer 58.

Claim 20

Independent claim 20 recites a method (carried out by the circuit of FIG. 5) for generating a third pulse sequence (CLOCK') in response to pulses of a periodic first pulse sequence (ROSC) having a period T_p comprising the steps of

a. generating each pulse of a second pulse sequence (CLOCK) in response to a separate pulse of the first pulse sequence (ROSC) with a first delay adjustable by first control data (SW(A)) with a resolution of T_p/N over a first range substantially wider than T_p/M, wherein M and N are differing integers greater than one **(specification paragraph 44 and carried out by device 54 of FIGS. 5 and 8);**

b. generating each pulse of the third pulse sequence (CLOCK') in response to a separate pulse of the second pulse sequence (CLOCK) with a delay adjustable by a second control data (SW(B)) with a resolution of T_p/M over a second range substantially wider than T_p/N **(specification paragraphs 42 and 43 and carried out by device 56 of FIGS. 5 and 7);** and

c. changing a magnitude of the first control data (SW(A)) and the second control data (SW(B)) in response to each pulse of the first pulse sequence (ROSC) such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner **(discussed at specification paragraphs 42 and 44 and carried out by device 58 of FIG. 5).**

Claim 34

Independent claim 34, best understood with reference to FIG. 4, recites a method for generating a third pulse sequence (CLOCK') in response to pulses of a periodic first pulse sequence (ROSC) having a period T_p, the method comprising the steps of:

a. generating each pulse of a second pulse sequence (CLOCK) in response to a separate pulse of the first pulse sequence

(ROSC) with a delay adjustable by first control data (SW(A)) with a resolution of T_p/N **(specification paragraph 44, carried out by device 54 of FIGS. 5 and 8);** and

b. generating each pulse of the third pulse sequence (CLOCK') in response to a separate pulse of the second pulse sequence (CLOCK) with a delay adjustable by a second control data (SW(B)) with a resolution of T_p/M **(specification paragraphs 42 and 43, carried out by device 56 of FIGS. 5 and 7);** and

c. changing a magnitude of the first control data (SW(A)) and the second control data (SW(B)) in response to each pulse of the first pulse sequence (ROSC) such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner, where M and N are relatively prime integers greater than one **(specification paragraphs 42 and 44, carried out by device 58 of FIG. 5).**

With M and N relatively prime as recited in claim 34, it is possible to adjust the repetitive control data patterns produced by programmable sequencer 58 to set the period of the output signal (CLOCK') with a resolution that is substantially higher than the delay resolution T_p/M or T_p/N of either the first or second means.

Grounds For Rejection To Be Reviewed On Appeal

Grounds For Rejection to Be Reviewed on Appeal are

1. whether claims 1-2, 4-8, 11, 20-21, 23-27, 30, 34-35 should be rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,255,790 (Hondeghem) in view of the document TTCrx Reference Manual (Christiansen), and

2. whether claims 3 and 22 should be rejected under 35 U.S.C. 103(a) as being unpatentable over Hondeghem and Christiansen in view of U.S. Patent 6,194,928 (Heyne).

Arguments

1. Arguments against rejection of claims 1-2, 4-8, 11, 20-21, 23-27, 30, 34-35 under 35 U.S.C. 103(a) as being unpatentable over Hondeghem in view of Christiansen.

Claims 1, 2, 4-8, and 11

Christiansen's FIG. 10 (the reference lacks page numbers) shows a two stage delay circuit (the reference lacks reference characters) that delays an input clock signal (in) to produce an output clock signal (out) by providing an adjustable number of delay elements (gates) in the signal path between in input and output signals. Each delay element of the first (coarse) delay stage provides a delay of T/N and each delay element of the second (fine) delay stage provides a delay of T/ (N-1). A separate multiplexer in each stage selects the number of delay elements the stage places in the signal path in response to input control data (sel).

The Examiner correctly points out at paragraph 5 of the Office Action dated 6/22/2006 that the applicant's "first means" and "second means" of claim 1 read on Christiansen's FIG. 10 which shows a delay circuit having first and second stages. The first stage includes a series of N delay elements receiving a periodic input signal (in), a multiplexer for selecting an output of one of the delay elements as a stage output signal, and a phase detector for setting the delay of each of the N delay elements to T_1/N where T_1 is the period of the input signal (in) to the first stage. The delay provided by the first stage depends on the value of the data input (sel) to the first stage multiplexer. For example, if the control data (sel) selects the output of the second delay element of the series, then the output

signal of the first stage will be delayed from its input (in) by $2(T_1/N)$, the sum of the unit delays of the first two delay elements. The resolution of Christiansen's first delay stage (the step size with which it can adjust its delay) will be T_1/N and the range (maximum delay - minimum delay) of the first delay stage will be $T_1-(T_1/N)$

The second delay stage is similar to the first delay stage except that it has only N-1 delay elements, each having a delay of $T_2/(N-1)$, where T_2 is the period of the input signal to the second stage, which is the output signal of the first stage. The range of the second stage is $T_2-(T_2/N)$.

If the control data (sel) values are fixed, then the period T_1 of input clock signal (in) to the first stage of the delay circuit of FIG. 10, and the period T_2 of the second stage input are the same. Thus we can let

$$T_1 = T_2 = T_p,$$

The resolution of the first stage is T_p/N,
The range of the first stage is $T_p - (T_p/N)$,
The resolution of the second stage is $T_p/(N-1)$ and
The range of the second stage is $T_p - (T_p/(N-1))$.

If we let $M = N-1$, then

The resolution of the first stage will be T_p/N,
The range of the first stage will be $T_p - (T_p/N)$,
The resolution of the second stage will be $T_p/(M)$ and
The range of the second stage will be $T_p - (T_p/M)$.

Thus the first and second stages Christiansen's circuit of FIG. 10 meet the limitations of the first and second means of claim 1, provided that the control input (sel) to both multiplexers of Christian's FIG. 10 <u>is held constant</u>. If the

control data input to the multiplexer of the first stage were to vary in a repetitive manner as recited in claim 1, then the range and resolution of the second stage becomes a function of the manner in which the control data varies.

Christiansen's FIG. 10 does not show the source of the control data (sel) to the multiplexers of the delay circuit of FIG. 1 but Christiansen's FIG. 4 depicts the context in which the delay circuit of FIG. 10 is used. Also Christiansen's paragraphs immediately proceeding and following FIG. 4 discuss the nature and source of the control data (sel) inputs to the multiplexers of FIG. 10. Christiansen's circuit of FIG. 4 is a receiver producing a pair of clock signals CLK01 and CLK02 of phase and frequency matching a clock signal in a remote transmitter. The receiver of FIG. 4 receives data arriving via a digital signal ("input from PINFET"). A "clock extraction" circuit of FIG. 4 monitors that digital input signal to determine the frequency of the clock signal the transmitter used to clock data onto the input signal and the receiver produces several output clock signals of that frequency. Some of the clock signals are provided to control timing in a "data decoder/demultiplexer" circuit which decodes the commands arriving on two data channels (A and B) of the input signal. The clock extraction circuit also supplies another clock signal to a pair of 'programmable fine deskew" circuits, each of which delays that clock signal by a separate amount to produce a separate one of output clock signals CLK01 and CLK02. Christiansen's FIG. 10 is provided as an example of either one of the two programmable fine deskew circuits of FIG. 4. Christiansen indicates (in the paragraph immediately preceding FIG. 4) that data for controlling the deskew circuits arrive via commands on the B channel of the input signal. As discussed in the section following FIG. 4, the control data is loaded into Coarse Delay and Fine Delay registers of the "control & interface" block of FIG. 4 which provides that data as input to the programmable fine deskew circuits for

controlling their delays. This, then, is the control data (sel) that controls the delay through the first and second stages of the delay circuit of FIG. 10.

The remote transmitter controls the frequency of the output clock signals CLK01 and CLK02 of the receiver circuit of FIG. 4 by setting the frequency of the clock signal it uses to clock data onto the "input from PINFET" signal, and controls the phase of each of the CLK01 and CLK02 signal by sending commands over the B channel to set the delays of the fine deskew circuits. Christiansen teaches to use commands arriving by the B channel to set the deskew delay "to compensate for the time necessary to transmit and decode … commands".
See the section "Coarse Delay" under Christiansen's heading "TTCrx internal registers".

Thus Christiansen's deskew circuit of FIG. 10 delays clock signals CLK01 and CLK02 to compensate for the inherent transmission line and processing delays in the path between the transmitter and receiver so that the CLK01 and CLK02 clock signals are of an appropriate phase. Christiansen does not teach that the transmission and processing delays in such a path vary in any repetitive manner, and one of skill in the art would conclude from Christiansen's teachings that once the control data input (sel) to the multiplexers of FIG. 10 is set to compensate for those path and processing delays, the sel data inputs to the multiplexers of FIG. 4 remain fixed in value and do not vary repetitively as recited in claim 1.

The Examiner, at paragraph 5 of the office action dated 6/22/2006, incorrectly asserts that Christiansen's FIG. 4 shows a "programmable sequencer for changing a magnitude of the first control data (SW(A)) and the second control data (SW(B)) in response to each pulse of the first pulse sequence (ROSC)" as recited in claim 1.

Note that in citing Christiansen as disclosing the programmable sequencer, the Examiner omits the limitation of

claim 1 that "the first and second control data vary repetitively in a programmable adjustable manner". Thus it appears that the Examiner is of the opinion that Christian's circuit of FIG. 4 shows a "programmable sequencer" but the programmable sequencer is not programmed to change the magnitude of the control data input (sel) to the multiplexers of the delay circuit of FIG. 10 so that they vary repetitively as recited in claim 1. However no programmable sequencer is shown in Christiansen's FIG. 4. The Examiner fails to indicate which part of FIG. 4 the Examiner thinks is a programmable sequencer and fails to point to any text in Christiansen suggesting that a programmable sequencer or any other kind of sequencer supplies the control data (sel) input to the multiplexers of FIG. 10. As discussed above, Christiansen teaches that the transmitter controls the data transmitted on the A and B channels of the input signal sets the delay control data to compensate for inherent delays in the signal transmission and data processing path. There is no suggestion in Christiansen's teaching that a programmable sequencer in the transmitter or anywhere else controls the control data (sel) input to the multiplexers of FIG. 4. Christiansen teaches that the sel data input to the multiplexers of Christiansen's FIG. 1 should be set to a <u>particular</u> value that provides the necessary delay for compensating for the inherent signal path and processing delay of the receiver. Once the delays are set to properly compensate for the inherent signal path and processing delays of the receiver, there is no reason to change the control data in the absence of any change to the signal path that would alter the path delay. Christiansen therefore provides no motivation for using a programmable sequencer or any kind of sequencer to provide the control data (sel) input to the multiplexers of FIG. 4. Note also as discussed above, varying the control input (sel) to the first stage multiplexer could cause Christiansen's second stage delay circuit to become unstable.

At paragraph 3 of the Office Action dated 6/22/2006 The Examiner cites Hondeghem FIG. 2 as teaching the recited "programmable sequencer (70, 84,112) for changing a magnitude of the first control data (116) and the second control data (118) in response to each pulse of the first pulse sequence (76) such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner" as recited in claim 1.

While clock signal 76 of Hondeghem's FIG. 2 is a "first pulse sequence", Hondeghem does not indicate the nature or purpose of signals conveyed on lines 116 and 118. Hondeghem does not teach that these lines convey control data and does not teach that devices 70, 84 and 112 change "a magnitude of the first control data (on line 116) and the second control data (on line 118) in response to each pulse of the first pulse sequence (on line 76)" as recited in claim 1. The Examiner points to FIGs. 2 and 3 as showing that data conveyed on lines 116 and 118 vary repetitively, but FIGs. 2 and 3 do not depict the behavior of signals conveyed on lines 116 and 118. The Examiner points to Hondeghem's col. 5, lines 1-57 as showing that data conveyed on lines 116 and 118 vary repetitively, but this section of Hondeghem says only that lines 116 and 118 connect device 112 to devices 108 and 110 and does not teach the nature or behavior of signals or data conveyed on those lines. The Examiner points to Hondeghem's col. 6, lines 20-57 as showing that data conveyed on lines 116 and 118 vary repetitively, but this section of Hondeghem says nothing at all about lines 116 and 118. Note that Hondeghem does not discuss the function of the devices 108 and 110 connected to lines 116 and 118 and that devices 108 and 110 of FIG. 2 apparently have inputs but <u>no outputs</u>. Hence the purpose and behavior of whatever signals or data may be conveyed on lines 116 and 118 cannot be deduced from the function of the devices 108 and 110 to which they are connected.

The Examiner at paragraph 6 of the Office Action dated 6/22/2006 incorrectly asserts that it would have been obvious to combine the teachings of Hondeghem and Christiansen. As discussed above, Christiansen discloses the first and second means recited in claim 1 but fails to teach a programmable sequencer or any other device for "changing a magnitude of the first control data and the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner" as recited in claim 1. Although Hondeghem discloses a CPU 70 (FIG. 2) that could conceivably be programmed to change values of data on lines 116 and 118 in response each pulse of a clock signal on line 76, Hondeghem does not teach that it should be so programmed.

In any case, even if Hondeghem were to teach that the data on lines 116 and 118 should vary repetitively, nothing in either Hondeghem or Christiansen suggests that the control data (sel) inputs to the multiplexers of Christiansen's FIG. 4 should be varied in a repetitive fashion, and one of skill in the art would not consider doing so, because doing so would render Christiansen's receiver circuit of FIG. 4 unfit for it's intended purpose, because Christiansen teaches away from this by teaching to set the sel data to particular values needed to compensate for path delays, and because varying the sel data input to the first stage multiplexer could cause the second stage to become unstable.

Thus the rejection of claim 1 under 35 U.S.C. 103(a) in view of Hondeghem and Christiansen was incorrect and should be withdrawn. Claims 2, 4-8 and 11 depend on claim 1 and are patentable over Christiansen for similar reasons.

Claims 20, 21, 23-27, 30, 34 and 35

Independent claims 20 and 34 each recite a step c of

"changing a magnitude of the first control data and the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner."

This is the function of the "programmable sequencer" of claim 1. Claims 20 and 34 are therefore patentable over the combination of Christiansen and Hondeghem for reasons similar to those discussed above in connection with claim 1. Dependant claims 21, 23-27, 30, 34 and 35 are further patentable over Christiansen and Hondeghem for similar reasons.

Claim 23 is additionally patentable over Hondeghem and Christiansen because it recites "the first and second ranges are each at least as wide as T_p." Hondeghem and Christiansen do not teach this. As discussed above, the range of Christiansen's first stage is $T_p - (T_p/N)$, and the range of the second stage is $T_p - (T_p/M)$. Since N and M are positive integers, the range of each stage is narrower than T_p. Hondeghem does not teach first and second delay means having ranges of any size.

Thus the rejection of claims 20, 21, 23-27, 30, 34 and 35 under 35 U.S.C. 103(a) in view of Hondeghem and Christiansen was incorrect and should be withdrawn.

2. Arguments against rejection of claims 3 and 22 under 35 U.S.C. 103(a) as being unpatentable over Hondeghem and Christiansen in view of U.S. Patent 6,194,928 (Heyne).

Claims 3 and 22

Claims 3 and 22 depend on claims 1 and 20, respectively. Since the Examiner relies on Christiansen and Hondeghem and not Heyne and as teaching the underlying subject matter of claims 1

and 20, claims 3 and 22 are patentable over the combination of Christiansen, Hondeghem and Heyne for reasons similar to those discussed above in connection with claims 1 and 20. Claims 3 and 23 further recite "at least one of said first and second ranges is wider than T_p". This limitation is not taught by Christiansen, Hondeghem or Heyne.

As discussed above, the range of Christiansen's first stage is $T_p - (T_p/N)$, and the range of the second stage is $T_p - (T_p/M)$. Since N and M are positive integers, the range of neither stage is wider than T_p as recited in claims 3 and 22.

Since Hondeghem does not teach the recited first and second delay means having ranges of any size, the Examiner correctly refrains from citing Hondeghem as teaching this.

Heyne teaches a delay unit T (FIG. 1) having a first delay means (comprising first delay elements I1 and multiplexer MUX1) for delaying an input signal IN to supply a signal to a second delay means (comprising second delay elements I2 and multiplexer MUX2) that further delays the signal to produce an output signal OUT. The Examiner indicates that Heyne's Abstract and col. 2, lines 4-47 teach that the range of either the first or the second delay means is greater than the period of the IN signal. However, although the Abstract teaches that the delay t_2 of each second delay element is greater than the delay t_1 of each first delay element, the Abstract contains no statement regarding the delay <u>range</u> provided by either the first or second delay means and contains no information from which delay range of either stage relative to the period of the input signal IN can be deduced. Heyne's col. 2, lines 4-47 teach the delay of unit T should adjusted by selecting the number of delay elements I1 and I2 in the signal path, but that section of Heyne contains no statement suggesting the delay <u>range</u> provided by either the first or second delay means is greater than the period of the IN signal or is in any way related to the IN signal period.

Heyne's col. 2 lines 48-55 teaches that the delay t_2 of each second delay element I2 is at least three times the delay t_1 of each first delay element I1, and that the number of delay elements in the signal path should be selected to compensate for temperature changes that affect the delay of the delay elements. However nothing in any cited section of Heyne contains any statement suggesting that the delay range provided by either the first or second delay means is greater than the period of the IN signal.

At paragraph 25 of the Office Action dated 6/22/2006 the Examiner suggests one of skill in the art would have been motivated to combine the teachings of Heyne with Christiansen and Hondeghem in order to "control fluctuations caused by temperature changes in the delay elements". The Examiner seems to be under the impression that the delay provided by each of Christiansen's delay elements of FIG. 10 is temperature dependant. However since the delay of Christiansen's delay elements of FIG. 10 is set by the phase detector to $1/N^{th}$ or $1/(N-1)^{th}$ of the period of the input signal (in) regardless of the temperature of the delay elements, the delay of Christiansen's delay elements does not vary with delay element temperature. Temperature fluctuations therefore do not affect the delay provided by Christiansen's delay circuit. Since Heyne teaches to solve a problem (delay variation due to temperature fluctuations) that does not exist in Christiansen's delay circuit of FIG. 10, the Examiner's stated motivation for combining Heyne with Christiansen and Hondeghem does not exist.

Thus the rejection of claims 3 and 22 under 35 U.S.C. 103(a) in view of Hondeghem, Christiansen and Heyne was incorrect and should be withdrawn.

Claims Appendix

1. An apparatus for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than period T_P, the apparatus comprising:

first means for generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a first delay adjustable by first control data with a resolution of T_P/N over a first range substantially wider than T_P/M, wherein M and N are differing integers greater than one;

second means for generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M over a second range substantially wider than T_P/N; and

a programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner.

2. The apparatus in accordance with claim 1 wherein M and N are relatively prime.

3. The apparatus in accordance with claim 1 wherein at least one of said first and second ranges is wider than T_P.

4. The apparatus in accordance with claim 1 wherein the first range is at least as wide as $(1 - 1/N)T_P$ and the second range is at least as wide as $(1 - 1/M)T_P$.

5. The apparatus in accordance with claim 4 wherein M and N are relatively prime.

6. The apparatus in accordance with claim 1 wherein the third pulse sequence is periodic.

7. The apparatus in accordance with claim 1

wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence,

wherein each first gate has a switching delay of T_P/N.

8. The apparatus in accordance with claim 1

wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence; and

wherein each second gate has a switching delay of T_p/M.

9. The apparatus in accordance with claim 8

wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

10. The apparatus in accordance with claim 9 wherein the second means further comprises means for monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

11. The apparatus in accordance with claim 1

wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence;

wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence;

wherein each first gate has a switching delay of T_P/N; and

wherein each second gate has a switching delay of T_P/M.

12. The apparatus in accordance with claim 11

wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

13. The apparatus in accordance with claim 12 wherein the second means further comprises means for monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

14. The apparatus in accordance with claim 13

wherein said plurality of first gates includes N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence;

wherein the switching delay of each of said first gates is controlled by a magnitude of the first control signal supplied as input thereto; and

wherein the first means further comprises means for

monitoring the first pulse sequence and the fifth pulse sequence and for adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

17. An apparatus for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than T_P, the apparatus comprising:

first means for generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a delay adjustable by first control data with a resolution of T_P/N;

second means for generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M;

a programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner,

wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse

sequence in response to pulses of the first pulse sequence,

wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence,

wherein each first gate has a switching delay of T_P/N, wherein each second gate has a switching delay of T_P/M,

wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence, and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

18. The apparatus in accordance with claim 17 wherein the second means further comprises means for monitoring the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

19. The apparatus in accordance with claim 18

wherein said plurality of first gates comprises N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence;

wherein the switching delay of each of said first gates is

controlled by a magnitude of a first control signal supplied as input thereto; and

wherein the first means further comprises means for monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence and for adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

20. A method for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than a period T_P, the method comprising the steps of:

a. generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a first delay adjustable by first control data with a resolution of T_P/N over a first range substantially wider than T_P/M, wherein M and N are differing integers greater than one;

b. generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M over a second range substantially wider than T_P/N; and

c. changing a magnitude of the first control data and the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control

data vary repetitively in a programmably adjustable manner.

21. The method in accordance with claim 20 wherein M and N are relatively prime.

22. The method in accordance with claim 20 wherein at least one of said first and second ranges is wider than T_P.

23. The method in accordance with claim 20 wherein the first and second ranges are each at least as wide as T_P.

24. The method in accordance with claim 23 wherein M and N are relatively prime.

25. The method in accordance with claim 20 wherein the third pulse sequence is periodic.

26. The method in accordance with claim 20

wherein step a comprises applying the first pulse sequence as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence; and

wherein each first gate has a switching delay of T_P/N.

27. The method in accordance with claim 20

wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence; and

wherein each second gate has a switching delay of T_P/M.

28. The method in accordance with claim 27

wherein step b comprises applying the first pulse sequence as input to M third gates connected in series so that the third gates generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by a magnitude of a control signal applied to all of the second and third gates.

29. The method in accordance with claim 28 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence; and

b2. adjusting the magnitude of the control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

30. The method in accordance with claim 20

wherein step a comprises applying the first pulse sequence

as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence;

wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence;

wherein each first gate has a switching delay of T_P/N; and

wherein each second gate has a switching delay of T_P/M.

31. The method in accordance with claim 30

wherein step b comprises applying the first pulse sequence as input to M third gates connected in series so that the third gates generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

32. The method in accordance with claim 31 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence; and

b2. adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse

sequence.

33. The method in accordance with claim 32

wherein said plurality of first gates comprises N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence;

wherein the switching delay of each of said first gates is controlled by a magnitude of a first control signal supplied as input thereto; and

wherein step a comprises the substeps of:

a1. monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence; and

a2. adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

34. A method for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than T_P, the method comprising the steps of:

a. generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a delay adjustable by a first control data with a resolution of T_P/N;

b. generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M; and

c. changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner, wherein M and N are relatively prime integers greater than one.

35. The method in accordance with claim 34

wherein step a comprises applying the first pulse sequence as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence;

wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence;

wherein each first gate has a switching delay of T_P/N; and

wherein each second gate has a switching delay of T_P/M.

36. The method in accordance with claim 35

wherein step b comprises applying the first pulse sequence

as input to M third gates connected in series so that the third gates
generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence; and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

37. The method in accordance with claim 36 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence; and

b2. adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

38. The method in accordance with claim 37

wherein said plurality of first gates comprises N first gates
connected in series and delaying the first pulse sequence to produce a fifth pulse sequence;

wherein the switching delay of each of said first gates is controlled by a magnitude of a first control signal supplied as input thereto; and

wherein step a comprises the substeps of:

a1. monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence; and

a2. adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

Evidence Appendix

None.

Related Proceeding Appendix

None.

Respectfully submitted,

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